REMARKS

Claims 1-27 are pending in the above-referenced application. In response to a restriction requirement imposed by the Examiner, the Applicant elects to prosecute Claims 1-16 without traverse. Claims 17-27 have been withdrawn from further consideration by the Examiner, 37 C.F.R. § 1.142(b), as being drawn to a non-elected invention. Claims 1-16 have been rejected by the Examiner. Claims 1 and 9 have been amended. Claims 28-32 have been added. The following remarks are directed to the claims as amended.

Election/Restrictions

The Examiner has required a restriction to one of the following two sets of claims under 35 U.S.C. § 121:

I. Claims 17-27, drawn to a method, classified in class 427, subclass 249.15; and
II. Claims 1-16 drawn to an apparatus, classified in class 118, subclass 728.

In response to the above restriction requirement, the Applicant elects to prosecute Claims 1-16 of Invention II, without traverse.

Rejection under 35 U.S.C. § 112 (2):

The Examiner has rejected Claim 9 under 35 U.S.C. § 112 (2) stating that "the phrase 'coating purity level of less than 1ppm' refers to low purity while low impurity would be desirable". The Applicant has amended Claim 9 to include the desirable language in the above phrase. Accordingly, Claim 9 is not now indefinite and reconsideration is respectfully requested.

Rejection under 35 U.S.C. § 102:

Claims 1-6 and 9-15 stand rejected under 35 U.S.C. §§102 (b) or 102 (e) as being allegedly anticipated by U.S. Patent No. 6,093,644 (Inaba). Examiner's grounds for rejection are hereinafter traversed, and reconsideration is respectfully requested.

In distinct contrast to Inaba, amended independent Claim 1 describes:

> A wafer boat for supporting silicon wafers, ----
> -----wherein the post coating surface finish of the wafer contact surface substantially prevents slip in the silicon wafers and is less than or substantially equal to 1 micron.

Inaba neither claims nor provides any support for a slip preventative post coating surface finish that is less than or substantially equal to 1 micron. The Examiner has stated that Col. 2, lines 52-55 disclose a surface finish having a maximum roughness of less than 10 microns and generally a roughness of 0.1 microns. The Examiner is only partially correct.

First of all, the 0.1 microns referred to by the Examiner has nothing to do with the maximum roughness of a surface finish. Rather, it is an indication of minimum particle sizes adhering to the surface. That is, as stated in the specification Col. 2, lines 53-54:

> "the number of particles having a **size of 0.1 microns or more and adhering to the surface".**

The Examiner is correct in that the specification does disclose:

> "a maximum surface roughness **Rmax,** which is maintained constantly at **10 microns or less** in n times of measurements" (Col. 2, lines 51-53).

However, no value or range of surface roughness is claimed in Inaba. Additionally and very significantly, Inaba only discloses support for a lower value of surface roughness of **3.2 microns or greater Rmax.** That is, the only reference to a lower roughness limit that can be found in the specification of Inaba is in Table II, Item No. 11 (and the footnote below the table, which states that "No. 11 corresponds to the present invention"). This limit fixes the support for the lower limit of surface roughness at 3.2 microns Rmax or greater. Accordingly, even if, for the sake of argument, Inaba had attempted to try to claim a surface roughness of less than 3.2 microns Rmax, the claim would have been rejected under 35 U.S.C. § 112 (1) for lack of enablement.

Just as importantly, the only support for any type of roughness range found in Inaba is in values of Rmax, while the Applicant's roughness ranges are specifically limited to values of Ra. This can be seen in Applicant's specification, page 5, paragraph 0014 wherein it states:

> "For purposes of this application all surface finishes will be designated in microns and shall represent the standard maximum roughness height index, i.e., arithmetic average, normally designates by the symbol Ra".

Inaba provides no support for any type of roughness range measured in Ra. In support of this, the Applicant has included with this Response a memorandum from Dick Hengst, a technical expert of the Assignee of this Application, i.e., Saint-Gobain Ceramics and Plastics, Inc. The memo states that:

> "There is no direct correlation between Rmax and Ra. Intuitively, Rmax must be greater than Ra, but even if Ra (which is a calculated average) is very low, one large irregularity on the surface could result in a large value of Rmax. Conversely, Rmax and Ra could also be relatively close."

Given that Inaba does not teach or suggest a post coating surface finish which is less than or substantially equal to 1 micron Ra, the Applicant is requesting that the rejection of Claim 1 be withdrawn.

However, if the Examiner wishes to repeat the rejection, than pursuant to MPEP 2144.03, the Applicant is requesting that the Examiner either take Official Notice or provide an Affidavit attesting that there is a correlation between Rmax and Ra. Additionally and more specifically, the Applicant requests that the Examiner take Official Notice or provide an Affidavit that a roughness value of 3.2 Rmax, as shown in Table II of Inaba, must correlate to a roughness value of 1.0 microns Ra. Moreover, if the Examiner should choose to take such Official Notice or provide such Affidavit, then further pursuant to MPEP 2144.03, the Applicant requests that the Examiner cite a reference in support of his position.

For at least the reasons stated herein above, the amended Claim 1 is patentable over Inaba. Claims 2-16, 28 and 29 should be allowable as variously depending from what should be an allowable independent Claim 1.

Rejection under 35 U.S.C. § 102:

Claims 7-9 stand rejected under 35 U.S.C. §103 (a) as being allegedly unpatentable over Inaba in view of U.S. Patent No. 5,904,778 (Lu). Additionally, Claim 16 stands rejected under 35 U.S.C. §103 (a) as being allegedly unpatentable over Inaba in view of U.S. Patent No. 6,171,400 (Wingo). Examiner's grounds for both rejections are hereinafter traversed, and reconsideration is respectfully requested.

As stated herein above, the amended Claim 1 is patentable over Inaba. Therefore Claims 7-9 and 16 should be allowable as variously depending from what should be an allowable independent Claim 1.

New Claims 28-32:

The new Claims 28-32 should be patentable over the cited prior art for the patentable subject matter they teach in and of themselves. In distinct contrast to the cited prior art, Claim 28 discloses:

A wafer boat having a post coating surface finish which substantially prevents slip in the silicon wafers (from Claim 1) and ---- "wherein the wafer contact surface is less than or substantially equal to 1/2 of the surface area of the wafer".

Additionally, in distinct contrast to the cited prior art, independent Claim 30 discloses:

A wafer boat --- "wherein the wafer contact surface is less than or substantially equal to 1/2 of the surface area of the wafer, and the post coating surface finish substantially prevents slip in the silicon wafer".

That is, the combination of a post coating surface finish that substantially prevents slip, and a wafer contact surface that has a maximum surface area of 1/2 the surface area of the wafer it supports, is not taught or suggested by the prior art.

A striking difference between Inaba and the Applicant's invention is that, even though they both claim surface finishes that are fine enough to prevent slip, the maximum acceptable surface finish of Inaba is at least ten times rougher than the maximum acceptable surface finish in the Applicant's invention (compare Inaba, Col 2, lines 51-53; with the Application, page 9, paragraph 0032). The reason for these seemingly contradictory assertions is that the wafer contact surface in Inaba is almost equal to the entire surface area of the wafer it supports. That is Inaba provides:

"a wafer loading face in the form of a plane to support the wafer by means of an extensive plan of the wafer loading face such that the formation of said slip line is prevented" (see Inaba, Col. 1, lines 30-32; and Fig. 1).

By increasing the ratio of the wafer support surface area to the surface area of the wafer itself, the weight of the wafer on the support surface is distributed over a much larger area and a much rougher surface finish can be tolerated. However, this can also lead to other problems, such as increasing the chances of scratching the backside of the wafers or limiting the ability of automated equipment to handle the wafers. For that reason, the exemplary embodiments of the wafer boats of the Applicant's invention have a wafer contact surface 38 that is far less than 1/2 the surface

area of the wafer itself (see Applicant's Fig. 3, wherein the wafer contact surface 38 is the top surface of the thin ceramic arms 32).

In support of the above, the memo from the Assignee of this Application, also states that:

> "With respect to supported surface area of the wafer, this is very critical. The relationship below best describes the situation.
>
> Stree (total) = Stress (gravitational) + Stress (frictional) + Stress (thermal)
>
> To minimize slip, one must minimize Stress (total). In our case, Stress (thermal) is considered to be constant. As the area supporting the wafer is decreased, the stress due to gravity increases. To maintain stress total below the threshold required to induce slip, the frictional stress must be minimized. It is also the desire of the end user to minimize the contact between the wafer support surface and the wafer. Although large support is better for minimizing gravitational stress (and therefore, slip), large contact on the backside can create problems down-stream in the semiconductor manufacturing process, reducing yield."

In view of the aforementioned, it is believed this application is now in condition for full allowance and such action at an early date is earnestly solicited.

It is believed that the foregoing remarks fully comply with the Office Action.

The Examiner is invited to contact Applicant's representative at the below-listed phone number with any questions.

Applicant believes no fee is due for this Response. However, should there be any deficiency in fees associated with the filing of this Response, please charge our Deposit Account No. 13-0235.

Respectfully submitted,

By Stephen P. Scuderi

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Version with Markings to Show Changes Made

A marked-up version of the amendments are shown below showing additions with underlining and deletions between brackets.

In the Claims:

The replacement Claims 1 and 9 as follows:

1. (Amended) A wafer boat for supporting silicon wafers, the wafer boat comprising:

a ceramic body having at least one wafer support structure sized to support a silicon wafer thereon;

a ceramic coating disposed on a surface of the wafer support structure, the ceramic coating having an impurity migration preventing thickness and a wafer contact surface, the wafer contact surface having a post coating surface finish;

wherein the post coating surface finish of the wafer contact surface substantially prevents slip in the silicon wafers and is less than or substantially equal to 1 micron.

9. (Amended) The wafer boat of Claim 1 wherein the ceramic coating has [a purity] an impurity level of substantially 1 ppm or less.

SAINT-GOBAIN
SEMICONDUCTOR

December 11, 2002

SEMICONDUCTOR COMPONENTS GROUP

Dear Stephen,

I would summarize the technical explanations as follows:

There is no direct correlation between Rmax and Ra. Intuitively, Rmax must be greater than Ra, but even if Ra (which is a calculated average) is very low, one large irregularity on the surface could result in a large value for Rmax. Conversely, Rmax and Ra could also be relatively close.

With respect to supported surface area of the wafer, this is very critical. The relationship below best describes the situation.

Stress (total) = Stress (gravitational) + Stress (frictional) + Stress (thermal)

To minimize slip, one must minimize Stress (total). In our case, Stress (thermal) is considered to be constant. As the area supporting the wafer is decreased, the stress due to gravity increases. To maintain stress total below the threshold required to induce slip, the frictional stress must be minimized. It is also the desire of the end-user to minimize the contact between the wafer support surface and the wafer. Although larger support is better for minimizing gravitational stress (and, therefore, slip), large contact on the backside can create problems down-stream in the semiconductor manufacturing process, reducing yield.

Please let me know if you have more questions or need additional explanations.

Dick Hengst

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